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Review Article

Sigma-Delta Modulators for Analog-to-Digital & Digital-to-Analog Conversion: A Review

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Abstract: Analog-to-digital and digital-to-analog converters manifest a very imperative role in many applications where data is interfaced with real analog world. The occurrence of some problems like jitter, quantization errors, integral nonlinearity and conversion time reduces the performance of both analog-to-digital (A/D) and digital-to-analog (D/A) converters. One of the most efficacious ways to combat these problems is the use of sigma-delta modulation. Sigma-delta modulators became very prominent due to their noise shaping characteristic in an analog-to-digital and digital-to-analog conversion. A fundamental structure, noise shaping techniques and different architectures of sigma-delta modulators along with comparative analysis are discussed in this review paper.

Keywords: Sigma-delta modulator (SDM), Multi-stage noise shaping (MASH), Oversampling ratio (OSR), Noise transfer function (NTF), Error feedback modulator (EFM).

1. INTRODUCTION

Sigma-delta modulation has a major contribution in high-resolution A/D and D/A converters. A higher SNR level is achieved during the conversion process which makes it a better choice to use in audio CD format. Its role is very predominant in wireless technologies such as long-term evolution advanced (LTE-Advanced), IEEE802.11ac, GSM and CDMA, etc where high-speed ADC's with wide bandwidth is necessary while reducing overall cost and glitch-induced harmonic distortion [1-6]. Other applications comprise instrumentation, seismic activity measurements, speech, video, ISDN, digital cellular radio, frequency synthesizer, chromatography, and biomedical applications [7-8].

Quantization noise is created during A/D and D/A conversion which leads to the improper reconstruction of the signal [9]. Sigma-delta modulator takes advantage of the technique called noise shaping along with oversampling is introduced to remove the noise from signal bandwidth and transfer it to a higher frequency region [10].

ΣΔ Modulator (SDM) is a two-block structure, the sigma (Σ) block and the delta (Δ) block [11]. The sigma (Σ) block consists of a feed-forward filter denoted by F (Z) followed by the quantizer (as shown in Fig.1). The feed-forward filter is combined with a feedback path to form a loop filter [12]. The output is subtracted from the input through negative feedback making it a delta block [13-14].

It must be remembered that the DAC is not implanted in the feedback path of ΣΔ modulators for a digital-to-analog converter (as shown in figure 2). The analysis to evaluate the output was performed in the z-domain. In Fig. 2, X (z) represents the input signal passed through the loop filter with a transfer function ($Z^{-1}/1-Z^{-1}$) and Y (z) indicates the output signal. The output for the first-order sigma-delta modulator can be written as:

$$Y(Z) = X(Z)\, Z^{-1}+(1-Z^{-1})E(Z) \quad (1)$$

The equation (1) is a combination of two functions. One is "Signal transfer function (STF)" and the other one is "Noise transfer function (NTF)". STF determines the matching behavior of its input signal to the output signal. The noise

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transfer function determines the noise shifting to a higher frequency region. The shape of the noise transfer function is such that it provides low response at lower frequencies and high response at higher frequencies like high pass filter as shown in Fig. 3. The output signal can be written as:

$$Y(Z)=STF(Z)X(Z)+ NTF(Z)E(Z) \quad (2)$$

From the above equation, it is concluded that:

$$STF\ (Z)=Z^{-1} \quad (3)$$

And

$$NTF\ (Z)=(1-Z^{-1}) \quad (4)$$

$$|NTF\ (e^{jw})|^2 = (2\ \sin(\omega/2))^2 \quad (5)$$

This article is prepared as follows. Section 2 discusses the research work that has already been carried out to develop different variants of sigma-delta modulators in the telecommunication industry. Section 3 analyses and compares the different architectures of sigma-delta modulators in terms of their characteristics, applications, advantages, and limitations in tabular forms. Section 4 represents the conclusions and future scope of this paper. Section 5 consists of references.

2. ∑Δ MODULATORS ARCHITECTURES

The engineers and scientists have taken a keen interest in SDM due to proper reconstruction of the original audio signal [15]. Scientists had developed different SDM architectures. These existing architectures are mentioned in Fig. 4. The important SDM architectures are explained below.

2.1 Single Quantizer Sigma-Delta Modulator (SQ-SDM)/ Traditional ΣΔ Modulator

Second-order and N^{th} order traditional sigma-delta modulators are also known as SQ-ΣΔ modulator [16-17]. It is represented in Fig. 5. The input is

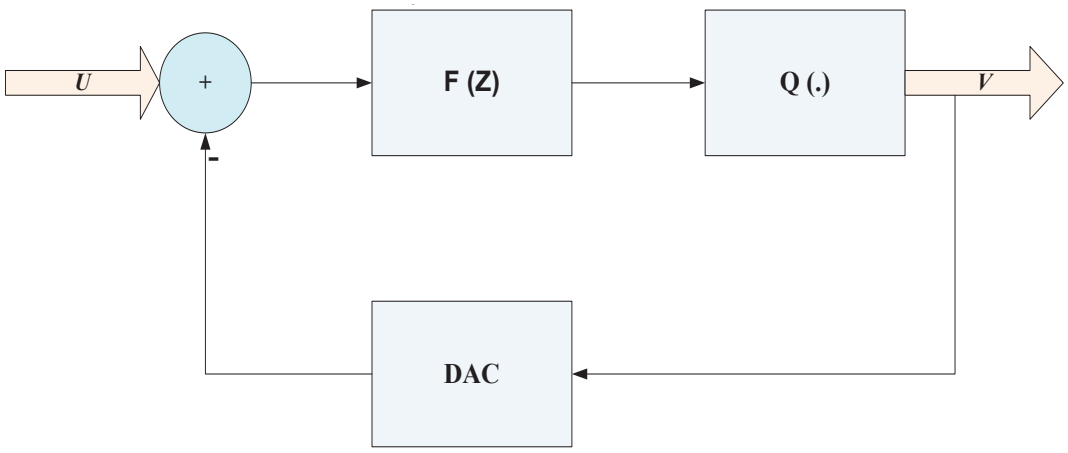

Fig 1. First-order sigma-delta modulator

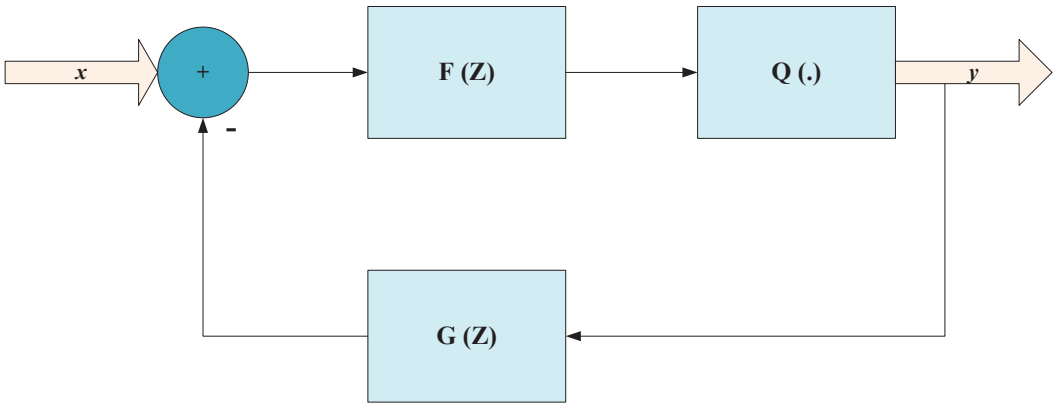

Fig. 2. First-order sigma-delta modulator for digital-to-analog converter

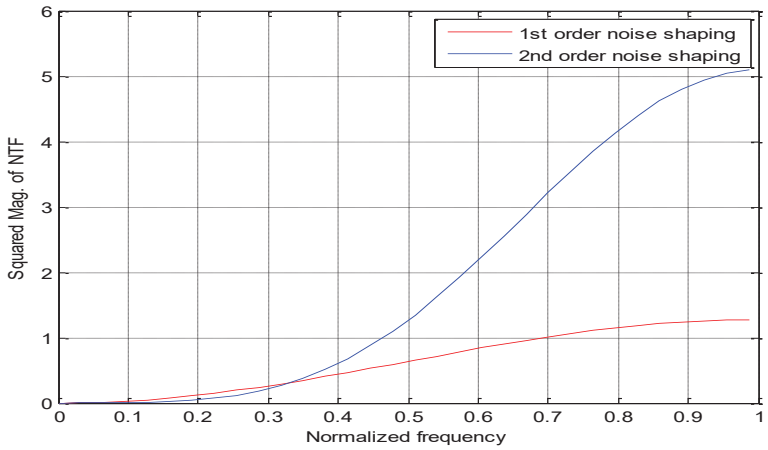

Fig. 3. 1st and 2nd order Noise shaping

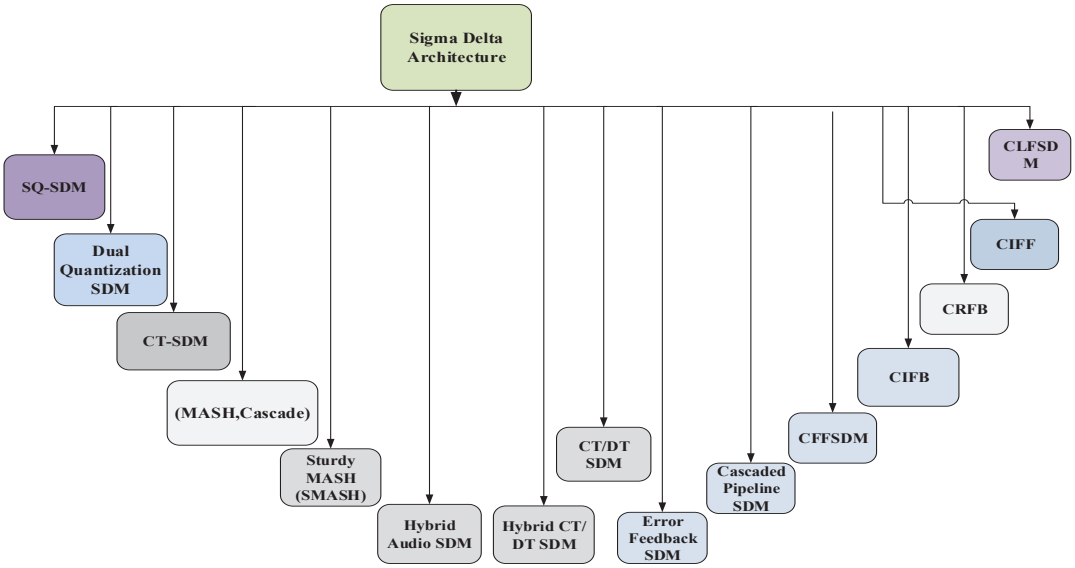

Fig. 4. Different architectures of sigma-delta modulator

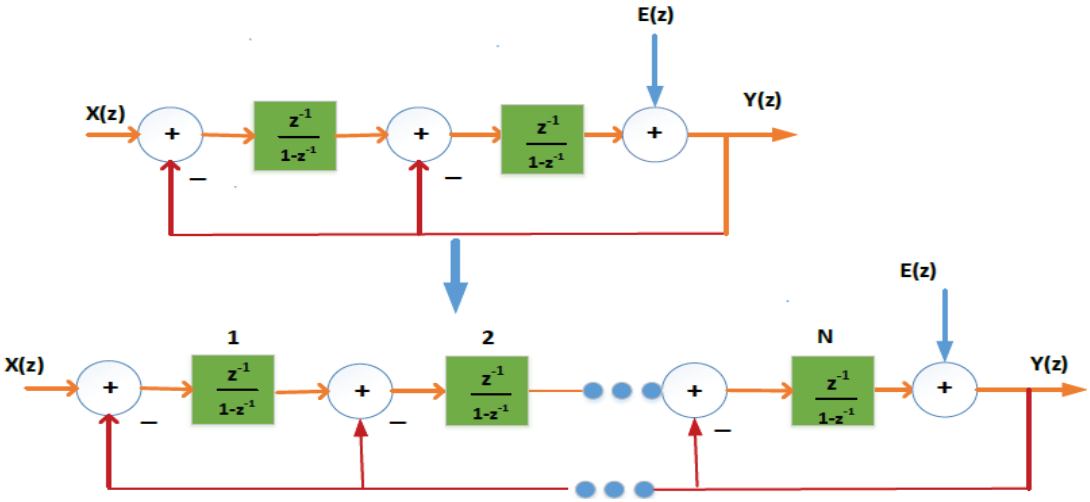

Fig. 5. Second order and nth order ΣΔ modulator (SQ-SDM)

passed through a feed-forward filter ($Z^{-1}/1-Z^{-1}$). The quantizer is located only at the last stage. The output signal is determined as:

$$Y(Z) = STF(Z)X(Z) + NTF(Z)E(Z) \quad (6)$$

The SQ-ΣΔ modulator type was further modified and named as "Reduced complexity single quantizer-sigma-delta modulator (RC SQ-ΣΔ modulator) [18]. RC SQ-ΣΔ modulator was implemented practically (by considering the effect of dithering). The quantizer is deployed in every stage of the architecture as shown in Fig. 6. The output Y (Z) can be expressed as:

$$Y(Z)=STF(Z)X(Z)+N_3(Z)+N_1(Z)+N_2(Z) \quad (7)$$

N_1, N_2, and N_3 represent the contribution of the filters of the first stage, second stage, and third stage quantizers.

2.2 Dual Quantization ΣΔ Modulator

This architecture includes two quantizers. One is known as a fine quantizer and the other is known as a coarse quantizer. They are placed in the feedforward and feedback paths respectively. The fine quantizer is responsible for generating NTF while the coarse quantizer produces a digital noise shaping loop (DNSL).

DNSL reduces the sensitivity between the analog and digital paths in this architecture. DNSL is an error feedback structure [19-20]. Dual quantization ΣΔ modulator consists of a chain of integrators with several feed-forward gains as shown in Fig. 7. The internal structure of the DNSL (first-order) is shown in Fig. 8.

2.3 Continuous-Time (CT)-ΣΔ Modulator

This architecture includes two quantizers. Sigma-delta modulator in the feedback path provides additional quantization. Most significant bits (MSB) are passed by the digital quantizer and truncate the other bits [21]. Dual quantization CT-ΣΔ modulator is presented in Fig. 9. Y_Q (Z) is the output of a digital sigma-delta modulator and is mathematically written as:

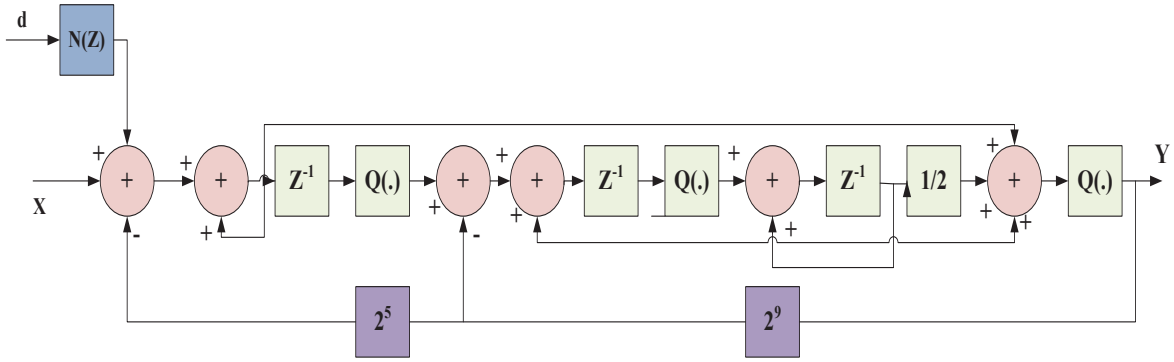

Fig. 6. RC third-order SQ-DΣΔ modulator

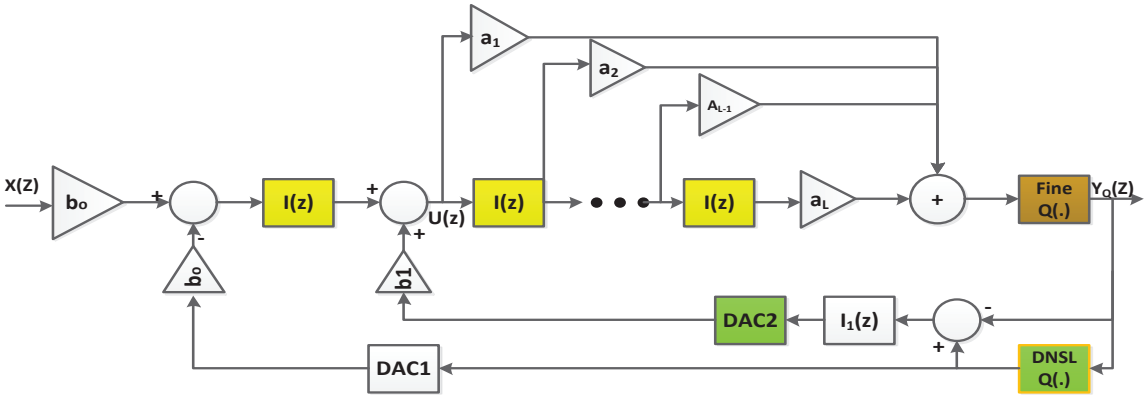

Fig. 7. Dual quantization SDM

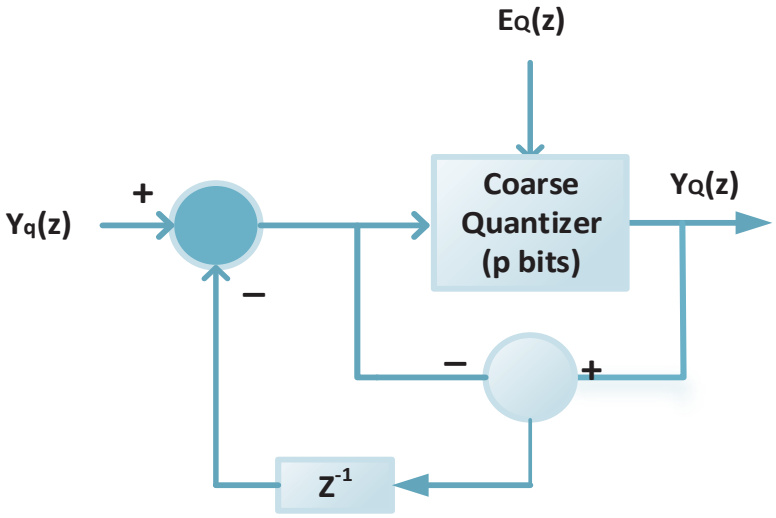

Fig. 8. First-order p-bit DNSL

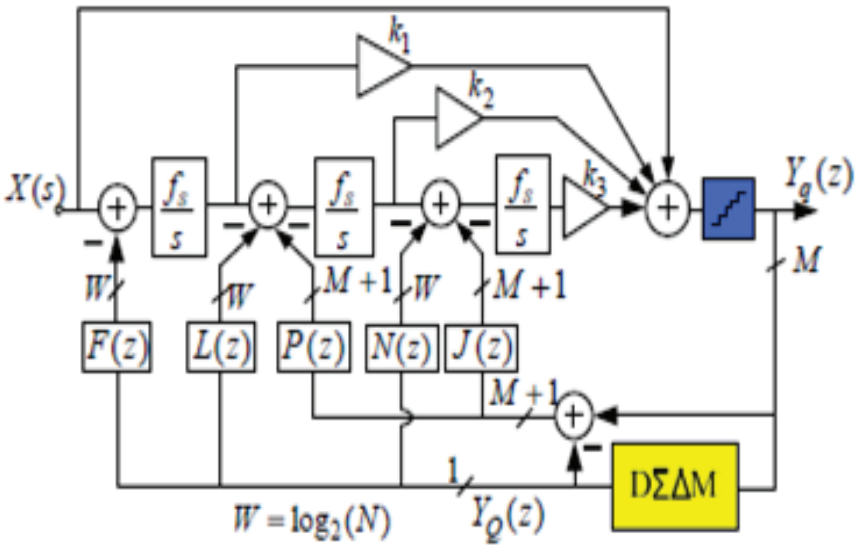

Fig. 9. Dual quantization CT-*ΣΔ* modulator

$$Y_Q(Z) = Y_q(z) + E_q(z)(1 - s(z)) \quad (8)$$

The dual quantization architecture decreases the bit length in the feedback path which increases clock jitter sensitivity. Spectrally shaped feedback is used to minimize the sensitivity of the clock jitter. The proposed architecture is displayed in Fig. 10.

2.4 Multi-Stage Noise Shaping (MASH, Cascade ΣΔ Modulator)

In multi-stage noise-shaping (MASH) architecture, the input is applied to the integrator which comprises accumulators and delay blocks. Then the signal from the integrator is fed to the quantizer. The quantized output is then fed back to the summer to subtract it from the input. The average output of the quantizer follows the average input. The second-order MASH consists of a combination of integrator and delay block in all the two stages with a single quantizer (as shown in Fig. 11). This architecture can be used in designing and implementing a high order, high accuracy ΣΔ modulator. This architecture helps in high signal-to-quantization noise ratio (SQNR), high signal-to-noise ratio (SNR), high dynamic range, and high spurious-free dynamic range (SFDR) [22-24].

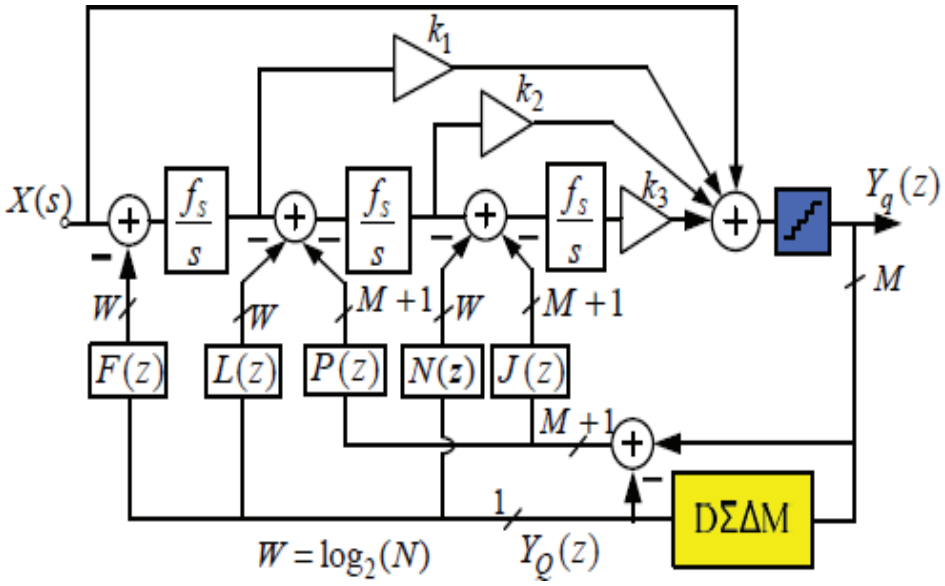

Fig. 10. Dual quantization CT-ΣΔ modulator with spectrally shaped feedback

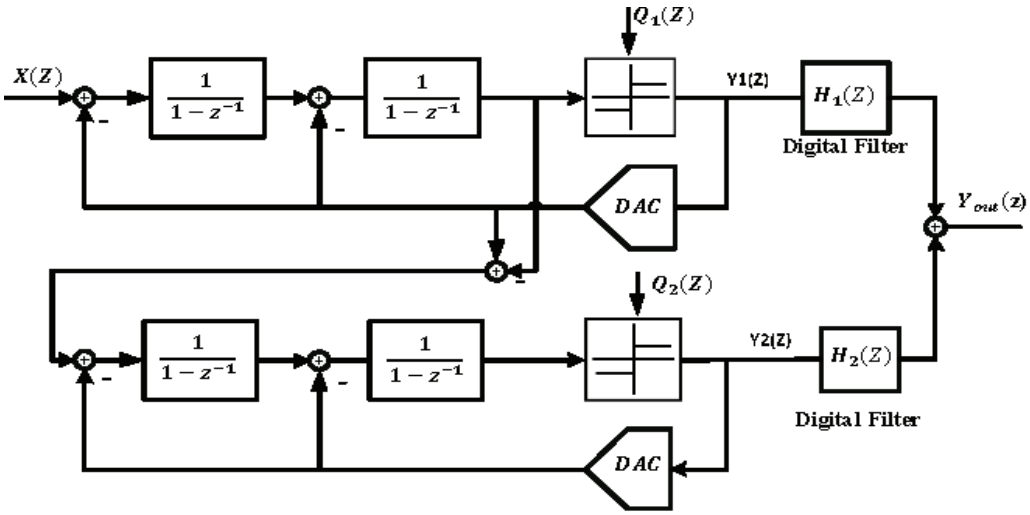

Fig. 11. MASH Sigma-delta modulator

2.5. Sturdy (SMASH) ΣΔ Modulator

The noise/signal power increases in MASH architecture, which results in saturation of the quantizer. It happened because the quantizer must process all the quantization noise in the signal. The above problem reduces the stability of the modulator and produces distortion. This problem was overcome by modifying conventional MASH architecture. This modification leads to a new architecture named "Sturdy multistage noise-shaping (SMASH)" [25-26]. The modification from MASH to SMASH is shown in Fig. 12. The NTF and STF are mathematically calculated by considering the output of SMASH.

$$Y_{SMASH} = STF_1X - NTF_1NTF_2E_2 + NTF_1(1-STF_2)E_1 \quad (9)$$

In eq. (9), STF_1 is the signal transfer function, NTF_1 and NTF_2 represent the first and second stage noise transfer function, E_2 is the error of the second stage. The error of the second stage is shaped by the two noise transfer functions NTF_1 and NTF_2. Here E_1 is the quantization noise of the first stage. Here E_1 is the quantization noise of the first stage. The value of STF_2 is determined as:

$$STF_2 = 1 - NTF_2 \quad (10)$$

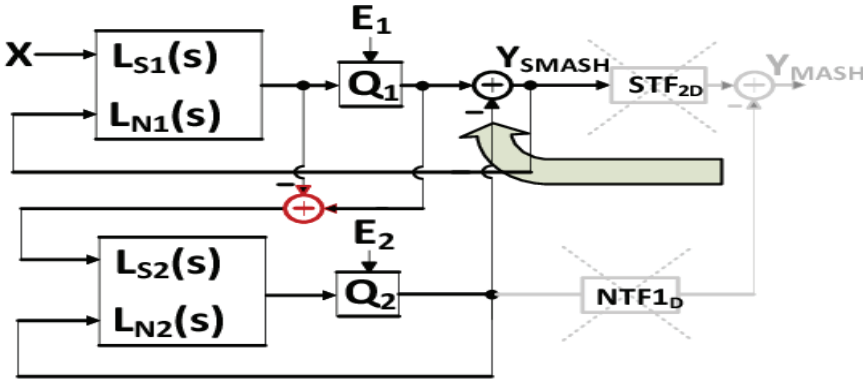

Fig. 12. Transformation of MASH architecture to SMASH

2.6. Cascaded Pipeline ΣΔ Modulator

Cascaded modulator architecture is represented in Fig. 13. A pipeline ADC is cascaded with a ΣΔ modulator. The noise in ADCs is removed by the noise shaping process in ΣΔ loop. Integrators must be provided with high gain to reduce the effect of noise in this architecture [27-29]. To employ ΣΔ modulator in DAC, DAC will be removed in the feedback path of ΣΔ loop.

2.7. CT/DT Cascaded ΣΔ Modulator

CT/DT (continuous-time/discrete-time) cascaded ΣΔ modulator is a combination of continuous-time and discrete-time *ΣΔ modulator*. In this architecture, the continuous-time *ΣΔ modulator* is implemented in the first stage and discrete-time in the second stage. CT ΣΔ modulator consists of two or more than two feed-forward paths [30]. Its design consists of state-space realization which completely explains the matching of digital and analog coefficients. It efficiently removes quantization noise from the output of the first stage [31]. It is shown in Fig. 14.

2.8. Cascaded Low Order Feed-Forward ΣΔ Modulator (CLFSDM)

Cascaded ΣΔ modulator plays a crucial role in ADC [32]. This architecture also consists of two stages. In the first stage, a single bit low order MASH ΣΔ modulator is implemented, while the second stage comprises of high order feed-forward ΣΔ modulator (FFSDM). The main idea to originate this type of architecture is that conventional MASH ΣΔ modulator has low quantization noise at lower frequencies and FFSDM has low quantization noise at higher frequencies. So, a new architecture (CLFSDM) is implemented which has both the characteristics of MASH and FFSDM. The blind-online digital calibration technique is used to improve SNDR [33]. Fig. 15 shows the architecture of CLFSDM [34].

2.9. Cascaded Feed-Forward SDM (CFFSDM)

This architecture consists of a quantizer (coarse quantizer) in the feedback path as shown in Fig. 16. The output "w" is given by:

$$w = v_1 + H_1 v_2 \tag{11}$$

This architecture reveals that the output of CFFSDM and FFSDM is the same. Some problems like pole errors, gain errors and coefficient variations were observed in the practical implementation of this architecture. Due to pole errors and gain errors, the NTF changes from the required NTF. And due to the deviation in coefficient parameters, the coarse quantization noise emanates through the feedback path [35]. Hence, the error correction scheme was also introduced in this architecture as shown in Fig. 17. Error correction scheme involves adaptive filter based on least mean square algorithm (LMS) along with dither. The dither signal also lessens the tone in the baseband signal.

2.10. Hybrid Audio ΣΔ Modulator

Hybrid audio ΣΔ modulator contains the analog integrator, SAR ADC, digital filter with Excessive loop delay (ELD) compensator, a feedback DAC,

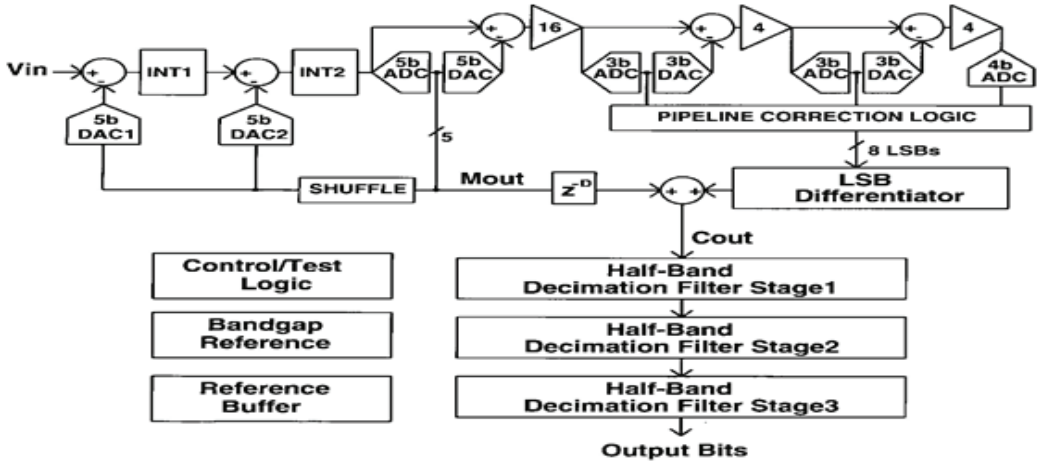

Fig. 13. Modified Cascaded pipeline architecture

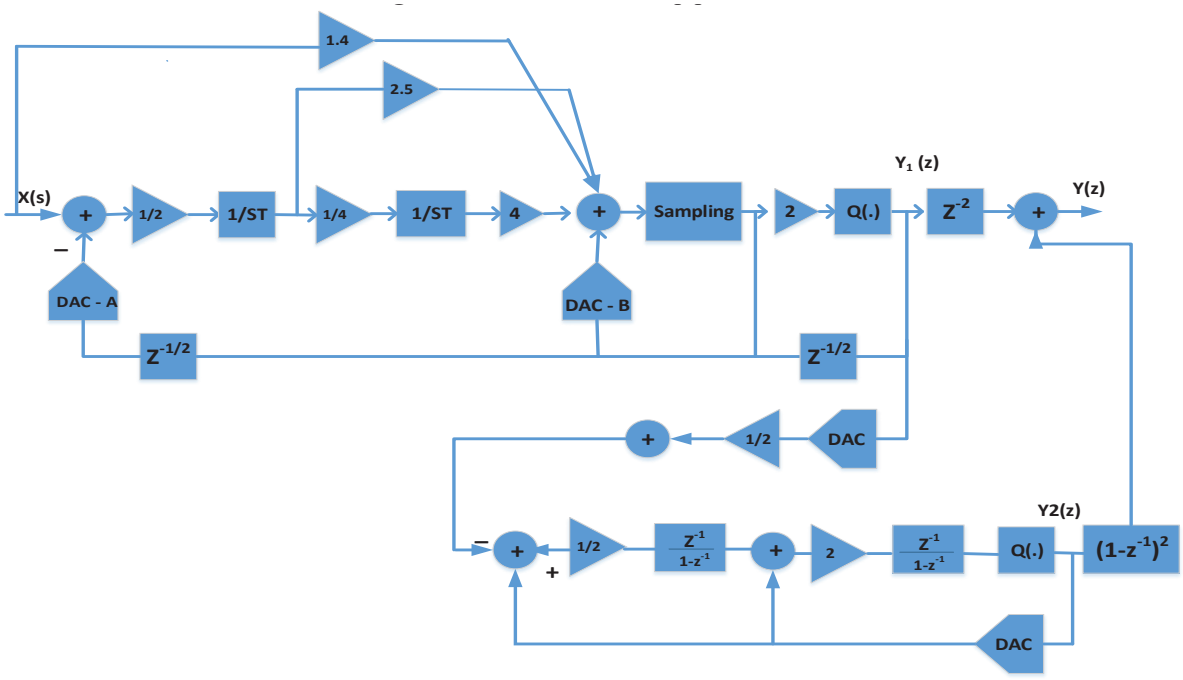

Fig. 14. Proposed CT/DT ΣΔ modulator

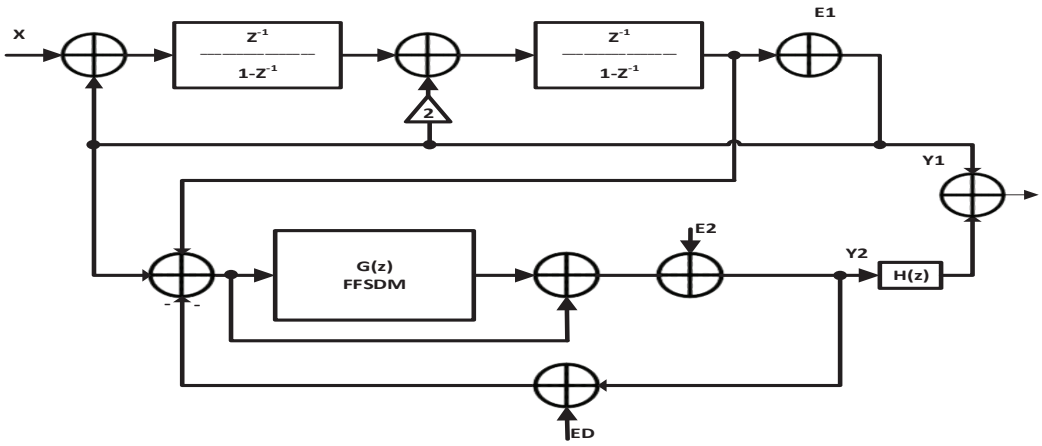

Fig. 15. Cascaded Low order Feed forward ΣΔ modulator

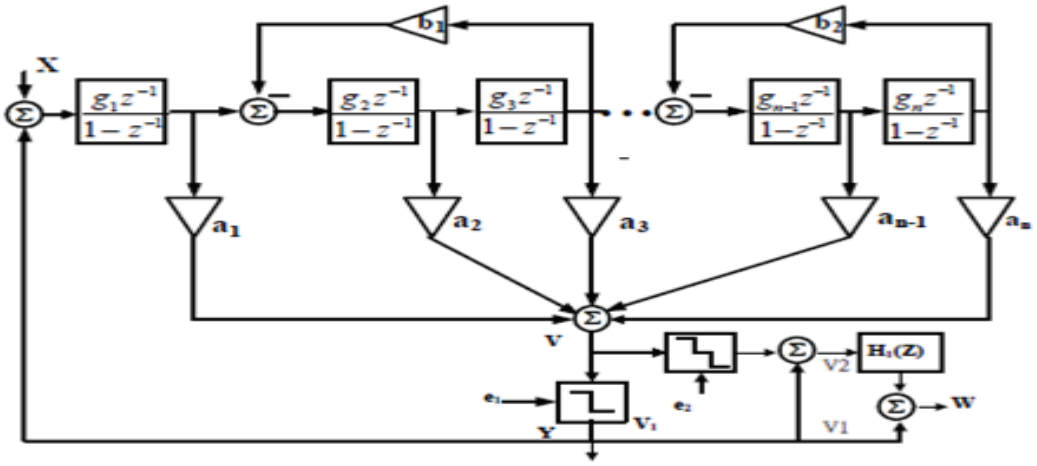

Fig. 16. Cascaded Feed forward ΣΔ modulator architecture without error correction

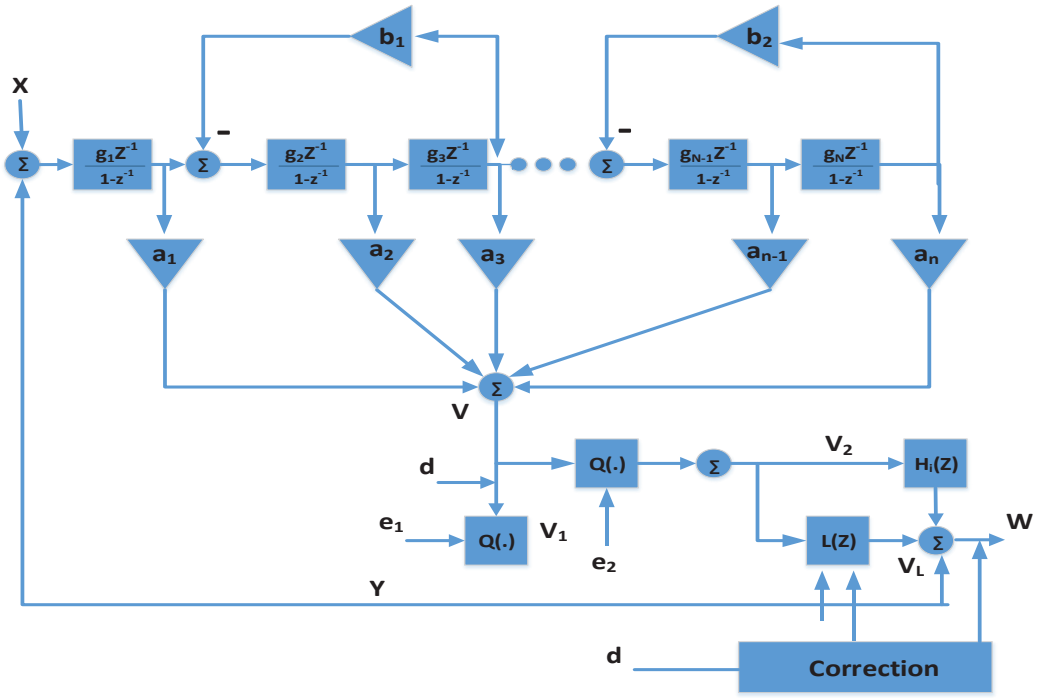

Fig. 17. Cascaded Feed forward ΣΔ modulator architecture with error correction

and a dynamic element matching (DEM) block as shown in figure 18[37]. Analog integrator is in the first stage and the second stage comprises the digital filters, DEM and DAC. The output of an analog integrator is converted into digital form by successive approximate registers (SAR). Bit by bit conversion is performed by the left channel when the right channel performs sampling and vice versa. Similarly, the other type of Hybrid ΣΔ modulator, which is a combination of continuous-time and discrete-time ΣΔ modulator named as "Hybrid CT/DT SDM", is displayed in Fig. 19.

After that, the multi-rate down sampling concept is effectively applied to this architecture to resolve the operation rate issue between continuous-time and discrete-time ΣΔ modulator. In this approach, the signal is efficiently downsampled in a cascade continuous-time ΣΔ modulator [38].

2.11. Dithered Hybrid MASH-EFM with Cancellation Transfer Function

MASH-EFM with dithering is another architecture that is a combination of transfer functions of MASH and EFM. The MASH transfer function is

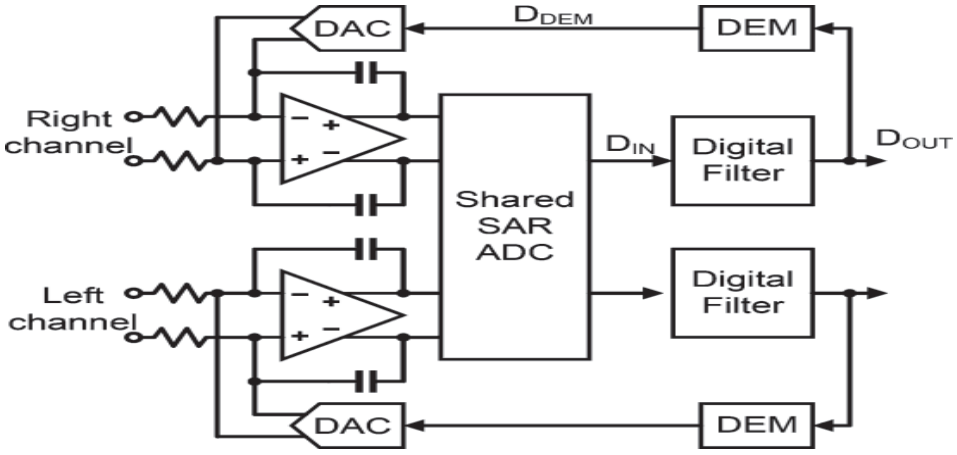

Fig. 18. Hybrid Audio ΣΔ modulator

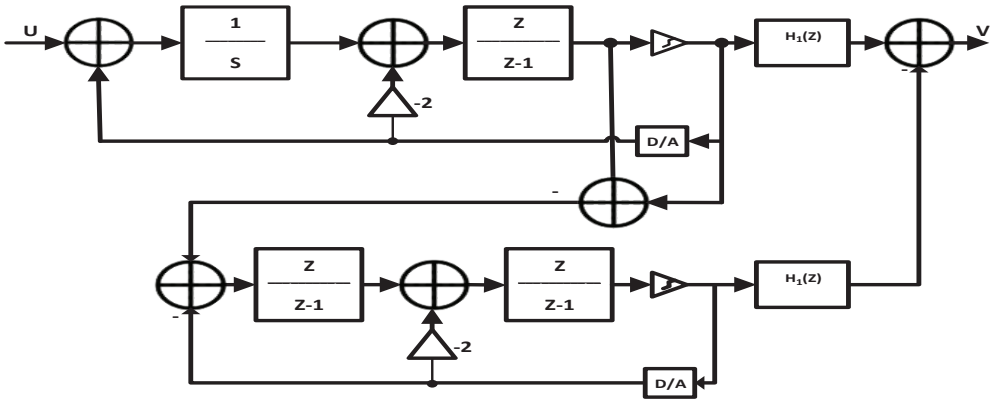

Fig. 19. Hybrid CT/DT SDM

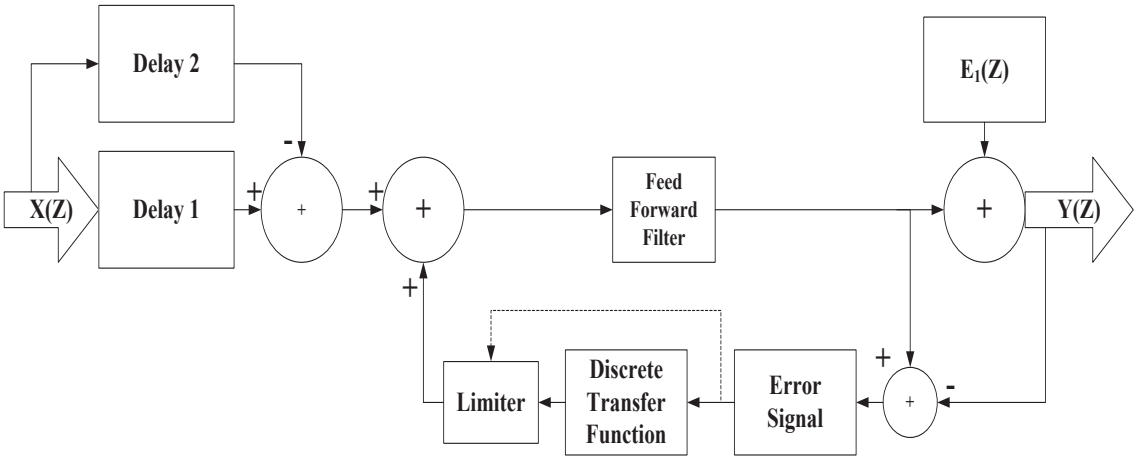

Fig. 20. Block diagram of 1st order Hybrid MASH-EFM architecture

implemented in the feedforward path and the EFM transfer function is placed in the feedback path [39].

2.12. Error Feedback Modulator (EFM)

In EFM, the error signal is fed back to the input signal while the working of other components of ΣΔ modulator is the same [40]. The architecture is shown below in Fig. 21. This architecture is more stable than any other ΣΔ modulator. EFM (DDSM) with bus-splitting schemes was also designed by the researcher and they also implemented its hardware [41]. The architecture is demonstrated in Fig. 22. The error feedback modulator was then modified to avoid the quantizer saturation using the limiter circuit [42].

2.13. Cascade-of-Integrators Feedback (CIFB)

In this architecture, the pole locations are adjusted to optimize the NTF. This is done by introducing gains in the feedback path. Hence, the modulator performance is enhanced by the poles only. Fig. 23 looks at this architecture. A lot of work has been done by the researchers to explore the insight of this architecture [43-47].

2.14. Cascaded Resonators with Distributed Feedback (CRFB)

This topology is introduced to minimize the In-band quantization noise by optimizing the coefficients of zeros of the NTF by the use of cascaded resonators with distributed feedback [48]. A 1-volt third-order CRFB ΣΔ modulator is implemented for audio DAC [49]. This architecture is also used as an ADC ΣΔ modulator [50]. The principle of this architecture is that the zeros of the NTF are defined by the local resonators and the poles are defined by the feedback gains. Fig. 24 represents CRFB in which "g1" is the local resonators and a1… ai are the feedback gains [51].

2.15. Cascade-of-Integrators Feed-Forward (CIFF)

In this architecture, some feedforward gains are used to feed the quantizer. It is used to optimize the NTF and STF both. The ADC CIFF contains DAC in the feedback path while DAC CIFF does not contain DAC in its feedback path. ADC CIFF is presented in Fig. 25. A time-sharing technique was also used in this architecture to avoid the use of extra active adders and critical timing issues [52].

Some more error correction techniques like dynamic element mismatching (DEM), Vector feedback mismatch shaping, and simple mismatch shaping are also implemented on these architectures to make them more efficient [53-58].

2.16. Incremental Feed-Forward Sigma-Delta Modulator

This architecture uses two discrete integrators in the feedforward path. FFSDM uses only one discrete integrator. The input and output signals of ΣΔ modulator and second discrete integrators respectively are added before the quantizer [59-60]. The architecture is shown in Fig. 26.

3. COMPARATIVE ANALYSIS OF DIFFERENT SDM ARCHITECTURES

Sigma-delta modulator consists of two major blocks, the low-pass filter, and the quantizer.

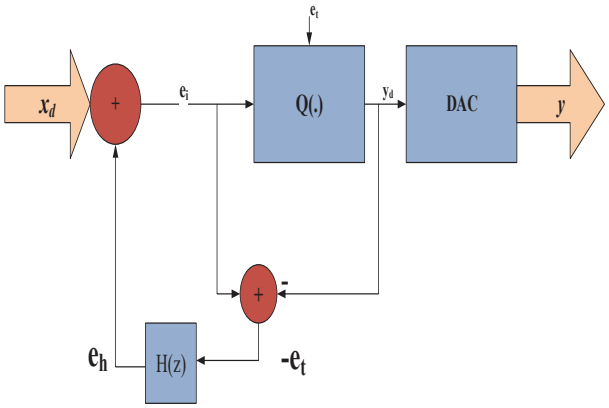

Fig. 21. Error Feedback modulator (EFM) architecture

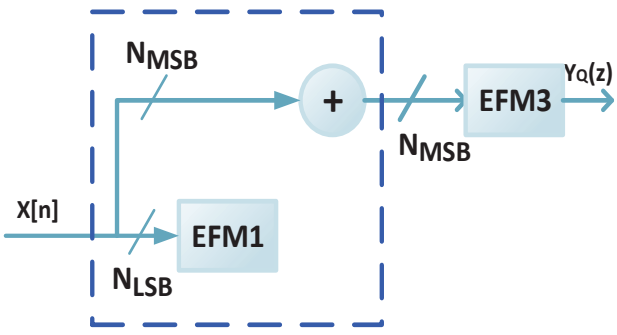

Fig. 22. 1-3 Bus splitting EFM3 architecture

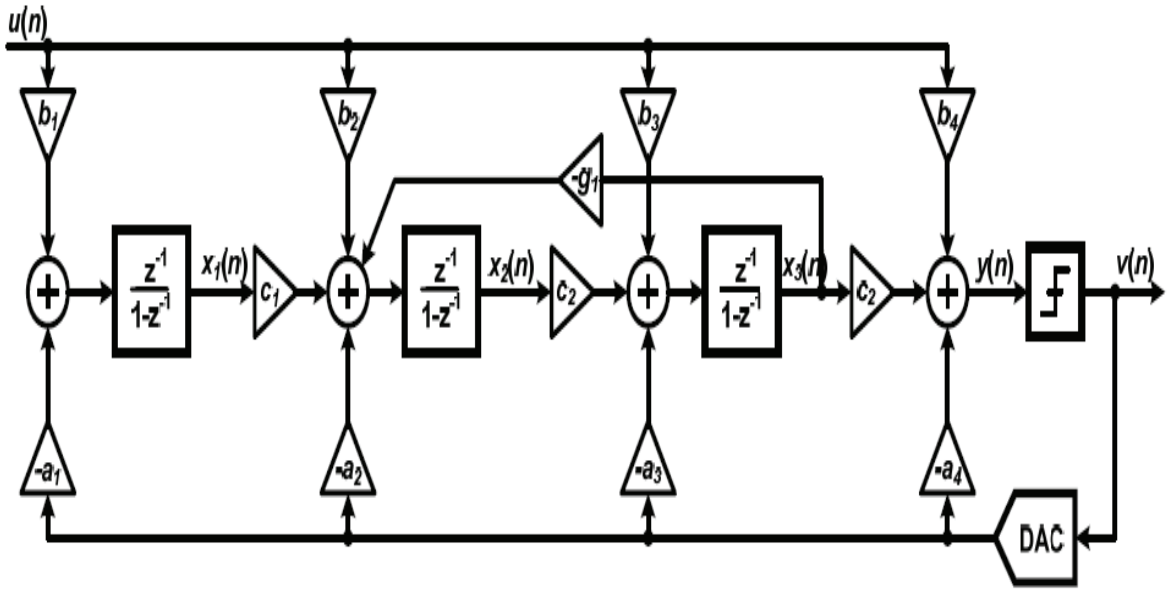

Fig. 23. CIFB architecture

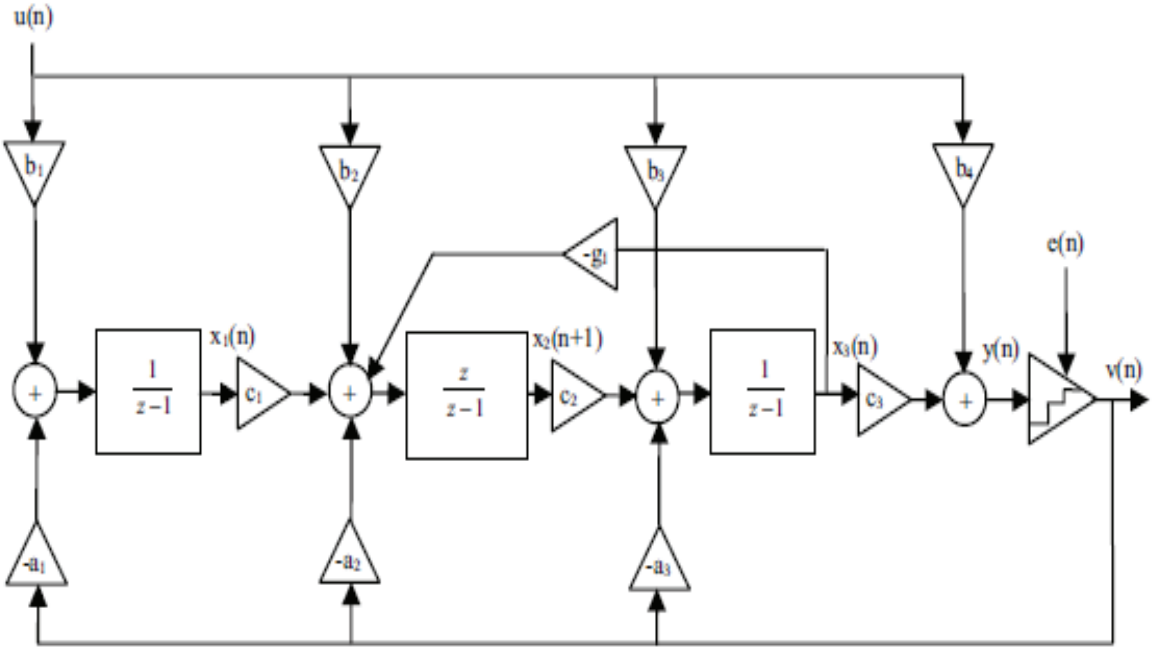

Fig. 24. CRFB ΣΔ modulator architecture

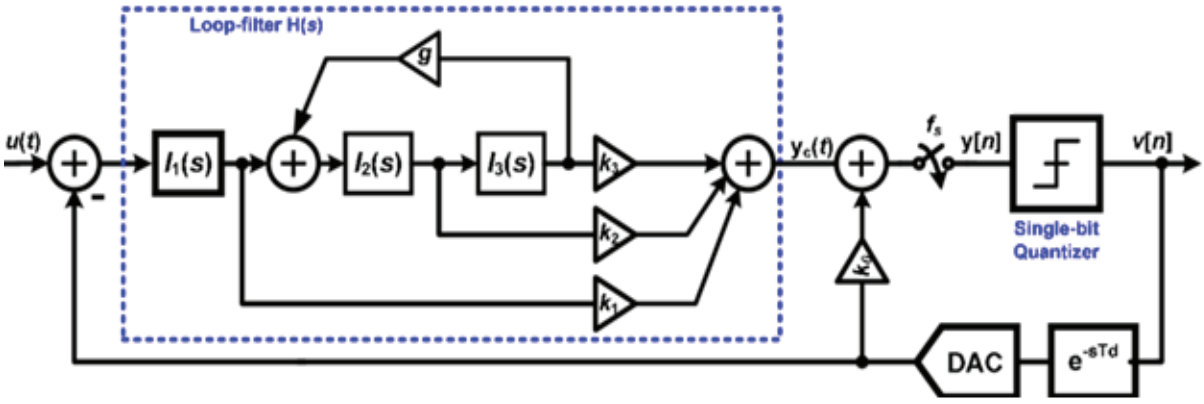

Fig. 25. CIFF ΣΔ modulator architecture

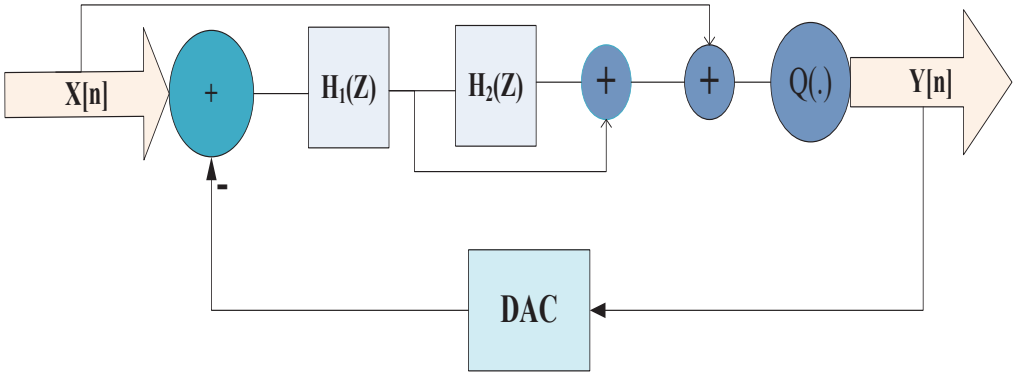

Fig. 26. 2nd order Incremental Feed forward ΣΔ modulator

Table 1. Summary of SDM architectures and their aspects

S. No.	References	SDM Paradigm	Characteristics and Applications
1	[17-18]	SQ-SDM	Used for low-resolution Telecommunication devices such as Super audio CD format and MP3.
2	[19-20]	Dual Quantization	Removes nonlinearity effects and mismatching errors in SDM. Used for low-resolution audio devices.
3	[22-24]	MASH	Provides high SNR with greater stability and used in the fractional-N frequency synthesizer
4	[25]	SMASH SDM	Eliminates all the problems that occurred in MASH architecture and can utilize for low voltage and high-resolution applications.
5	[26-29]	Cascaded pipeline SDM	Operates effectively in limited DC gain and under the maximum swings of input.
6	[31]	CT/DT Cascaded SDM	Operates efficiently at very high sampling frequencies and remove clock jitter. It is used for high resolution and Wideband applications.
7	[32-33]	Cascaded Low order Feed forward SDM (CLFSDM)	Reduces quantization noise over the whole frequency spectrum and hence increases SNDR.
8	[35]	Cascaded Feed forward SDM (CFFSDM)	Obtains high SNDR by reducing the non-linearity effect with the help of an adaptive filter and is suitable for wide bandwidth applications.
9	[37]	Hybrid CT/DT SDM	Combines the characteristics of CT and DT SDM. The MEMS-based accelerometer is an application.
10	[40-41]	Error feedback modulator (EFM)	The most stable architecture of SDM because it provides stability for time-varying inputs also. It is widely used in N-fractional PLLs.
11	[43-46]	Cascade-of-Integrators Feedback (CIFB)	Improves NTF by the modification of poles and is used for low-power applications.
12	[48-51]	Cascaded Resonators with Distributed Feedback (CRFB)	Removes In-band Quantization noise and is extensively used for audio applications such as embedding Headphone drivers.
13	[59]	Incremental Feed forward Sigma Delta modulator	Removes all types of noises with greater stability and is used in sensors.

Table 2. Limitations of SDM architectures

S. No.	References	SDM Paradigm	Limitations
1	[16]	SQ-SDM	Unstable for high-resolution applications and provides low accuracy.
2	[21]	Dual Quantization	Always requires spectrally shaping feedback to improve clock jitter insensitivity.
3	[25]	MASH	Causes saturation to the quantizer. Limited DC gains of OP-Amps create mismatching.
4	[25]	SMASH	Sturdy MASH suffers from instability as its order increases.
5	[33]	Cascaded pipeline	Requires to remove the effect of analog imperfection in the implementation.
6	[38]	CT/DT Cascaded	Increases complexity as continuous-time and discrete-time sigma-delta modulators are not compatible with each other
7	[33]	Cascaded Low order Feed forward SDM (CLFSDM)	Realization of the analog filter is complicated
8	[42]	Error Feedback modulator (EFM)	Requires limiter circuit to prevent the quantizer from overloading which increases circuit complexity.
9	[44]	Cascade-of-Integrators Feedback(CIFB)	It requires high power and chip area.
10	[53]	Cascade-of-Integrators Feedforward (CIFF)	Introduces critical timing issues.

The low-pass filter is designed according to the requirements of the desired application. Therefore, the low-pass filter designed for the low-resolution Telecommunication devices cannot be used for the GSM devices. Similarly, the design of the quantizer depends upon the requirements of the bits used for the specific application. Therefore, the quantizer designed for the low-resolution devices is not suitable for the wideband and high-resolution devices which use more than 16-bits in their architectures. Hence, every ΣΔ modulator architecture has different aspects and features. For instance, SQ-SDM was specifically designed for low-resolution Telecommunication devices such as super audio CD format. This type of ΣΔ architecture cannot be used for cryptography. Therefore, different ΣΔ modulators fulfill different requirements of various applications. The comparison based on characteristics and applications between different architectures is summarized in table 1. Some limitations have also been observed in ΣΔ modulators and are recapitulated in Table 2. For example, CIFB architecture uses various gains in a feedback loop. The adequate use of the different gains increases the circuit complexity. Hence, increases the chip area to occupy these gains.

4. CONCLUSION AND FUTURE SCOPE

The conventional analog-to-digital and digital-to-analog converters cannot remove the quantization noise which results in the performance degradation of converters. Sigma-delta modulator uses oversampling and noise shaping which efficiently removes the quantization noise from the signal bandwidth. Hence, they acquire high-performance parameters. The above study has presented those different architectures of sigma-delta modulators which are widely used in numerous applications in the telecommunication industry due to their stability and efficiency. Every architecture has its characteristics and applications. The characteristics, applications, and limitations are briefly presented in this review paper.

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